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Register Number:

DATE: 21-04-2017

**ST. JOSEPH’S COLLEGE (AUTONOMOUS), BENGALURU-27**

**SEMESTER EXAMINATION – APRIL 2017**

**B.Sc. Electronics – IV Semester**

**EL415: Verilog HDL**

**Time: 1 Hour and 30 Minutes Max. Marks: 35**

Note: The question paper has three parts and two printed pages.

**PART – A**

**Answer any THREE of the following 03X05=15**

1. a. What is a module? Discuss the four levels of design abstraction used in a module.

b. Declare the following variables in Verilog:

i. An 8-bit vector net called bus A.

ii. Decimal number 99 as a sized 8-bit number in binary.

iii. A memory MEM containing 256 words of 8 bit each.

iv. A 16 bit storage register called address. Bit 15 must me MSB. Store the value of register to a 16 bit decimal number equal to 10. (3+2)

2. a. Discuss any two System tasks used in verilog HDL.

b. Discuss delays in gates with a proper example. (2+3)

3. Explain blocking and non blocking assignments used in behavioural modeling with proper examples.

4. a. Write a note on Delay based timing controls.

b. Do the logical synthesis of the following modules and draw its output RTL diagram:

y= (~(X0^Y0)&~(X1^Y1)); (4+1)

5. What is structured modeling? Explain with a proper example.

**PART – B**

**Answer any THREE of the following 03X06=18**

6. Write a design (gate level) and test module for 4X1 multiplexer.

7. Write a design module and test module for JK flip flop using behavioral modeling.

8. The expression **assign #10 out = i1&i2;** is simulated using the following conditions. Write a test module and draw timing diagram to realize the output.

Conditions: i1 = 0; i2 = 0;

#20 i1 = 1; i2 = 1;

#40 i1 = 0; i2 = 1;

#20 i1 = 1; i2 = 1;

#05 i1 = 0; i2 = 1;

#10 $finish;

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9. a. Write a module using always statement to design a clock with time period = 10 and duty cycle = 40%. Initial value of clock = 0.

b. Write a module using repeat loop to delay the statement a = a+1 by 20 positive edges of clock.

10. Write a design and test module to realize a 4-bit ripple carry counter using behavioural modeling.

**PART – C**

**Answer any TWO of the following 02X01= 02**

11. reg A;

reg [1:0] B,C;

reg [2:0] D;

A = 1’b1; B = 2’b00; C = 2’b10; D = 3’b110;

What will be the result of the following expression:

Y = {4{A}, 2{B}, C};

12. Verilog is a concurrent programming language. Justify.

13. What is meant by the statement, “Continuous assignments are always active.”

14. Write one difference between functions and tasks.